

ATVA 2015, 13th International Symposium on Automated Technology for Verification and Analysis

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October 12–15, 2015, Shanghai, China http://atva2015.ios.ac.cn/

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KEYNOTES

Dino Distefano (Facebook & Queen Mary Uni. of London, UK) Joost-Pieter Katoen (RWTH Aachen University, Germany) J Strother Moore (University of Texas-Austin, USA)

BACKGROUND

The purpose of ATVA is to promote research on theoretical and practical aspects of automated analysis, verification and synthesis by providing a forum for interaction between the regional and the international research communities and industry in the field.

SCOPE

ATVA 2015 solicits high-quality submissions in areas related to the theory and practice of automated analysis and verification of hardware and software systems. Topics of interest include, but are not limited to:

- Formalisms for modeling hardware, software and embedded systems
- Specification and verification of finite-state, infinite-state and parameterized systems
- Program analysis and software verification
- Analysis and verification of hardware circuits, systems-on-chip and embedded systems
- Analysis of real-time, hybrid, priced/weighted and probabilistic systems
- Deductive, algorithmic, compositional, and abstraction refinement techniques for analysis and verification
- Analytical techniques for safety, security, and dependability
- Testing and runtime analysis based on verification technology
- Analysis and verification of parallel and concurrent hardware/software systems
- Verification in industrial practice
- Applications and case studies

Theory papers should preferably be motivated by practical problems, and applications should be based on sound theory and should solve problems of practical interest.

IMPORTANT DATES

April 22, 2015	Abstract submission deadline (AOE)
April 25, 2015	Paper submission deadline (AOE)
May 5, 2015	Submission of workshop proposals
Jun 8, 2015	Paper acceptance/rejection notification
Jun 10, 2015	Announcement of the accepted papers
July 5, 2015	Camera-ready copy deadline